REMARKS/ARGUMENT

Claims 1-9 and 11-14 stand allowed.

Claims 16 and 17 have been amended to overcome the Examiner's objection.

Claims 10 and 15-19 stand rejected under 35 U.S.C. 102(b) as being anticipated by Jones et al. (5,920,808). Applicants respectfully traverse this rejection, as set forth below.

In order that the rejection of Claims 10 and 15-19 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." Verdegall Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 10, as amended, requires and positively recites, a digital modulator for use in a radio frequency transmitter, comprising: "a phase-lock-loop (PLL) loop producing as an output signal a modulated RF signal", "a phase demodulator having an input port for **receiving unmodified the modulated RF signal** and having an output port for providing a phase information signal" and "a comparator having a first input port for receiving the **unmodified modulated RF signal** and having an output port for providing a phase information signal."

In contrast, the Jones reference shows in Figure 2 the 22.4 MHz signal output from PLL 237 (what the Examiner has equated to Applicants' modulated RF signal). Digital demodulator 125 performs a digital quadrature demodulation of the digital signals and outputs the in-phase and quadrature component signals at 22.4 Msps (col. 6, lines 26-29 & col. 9, lines 13-16). The digital decimator 229 receives the output signals of the digital quadrature demodulator 125 and performs a decimation by a factor of twenty-eight to produce 800 ksps complex base band signals (col. 9, lines 28-32). As such, Jones does not teach or suggest that digital decimator is "a phase demodulator having an input port for **receiving unmodified the modulated RF signal** and having an output port for providing a phase information signal", as required by Claim 10.

Further, trainer 131 receives the outputs from digital decimator 229. As such, Jones fails to teach or suggest that trainer 131 is "a comparator having a first input port for receiving the **unmodified modulated RF signal** and having an output port for providing a phase information signal", as further required by Claim 10. Accordingly, the 35 U.S.C. 102(b) rejection of Claim 10 over Jones is improper and should be withdrawn.

Independent Claim 15 requires and positively recites, a radio frequency (RF) modulator comprising: "a phase-lock-loop (PLL) loop **including a loop filter** and receiving as an input signal a modulation signal and producing as an output signal a modulated RF signal", "circuitry for producing an injection modulation signal", "circuitry for injecting the injection modulation signal into the phase lock loop **at a point before the loop filter**" and "control circuitry, coupled to the circuitry for injecting the injection modulation signal, for controlling the amplitude of the injection modulation signal".

Independent Claim 18 requires and positively recites, a method of producing phase shifts in a modulated RF signal, comprising the steps of: "producing an injection modulation signal", "injecting the injection modulation signal into a phase lock loop

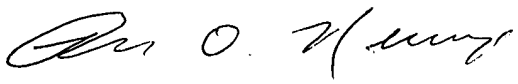
having a loop filter at **a point before the loop filter**" and "producing a modulated RF signal as an output from the phase lock loop".

In contrast, Jones fails to teach or suggest a PLL having a loop filter. As such, Jones fails to teach or suggest, "a phase-lock-loop (PLL) loop **including a loop filter** and receiving as an input signal a modulation signal and producing as an output signal a modulated RF signal" and "circuitry for injecting the injection modulation signal into the phase lock loop **at a point before the loop filter**", as required by Claim 15, and "injecting the injection modulation signal into a phase lock loop having a loop filter at **a point before the loop filter**", as required by Claim 18. The Examiner has not considered all of the words of Claims 15 and 18. As such, the 35 U.S.C. 102(b) rejection of Claims 15 and 18 is improper and should be withdrawn.

Claims 16 & 17 depend (directly or indirectly) from Claim 15 and are therefore similarly allowable. Claims 19 & 20 depend (directly or indirectly) from Claim 18 and are therefore similarly allowable.

Claims 1-9 and 11-14 stand allowed. Claims 10 and 15-20 stand allowable over the references of record. Applicants respectfully request allowance of the application as the earliest possible date.

Respectfully submitted,



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